ECUcore-5484

Focusing on applications that require a high degree of embedded computing power, the ECUcore-5484 combines a fast CPU, a performance optimized memory layout with a variety of communication interfaces. It targets applications that combine the need for high-speed data acquisition and realtime communication, such as Ethernet POWERLINK.

Feature Overview

Controller	Freescale MCF 5484 with ColdFire V4e Core
System Clock	200 MHz
RAM	64MB DDR-SDRAM (128MB optional)
Flash	16MB NOR (32MB optional)
EEPROM	32kB SPI (2kB optional)
Ethernet	2x 10/100 Mbps, 1x on-board PHY
CAN / UART	2 / 4
Others	SD-Card interface, RTC, Temperature sensor
I/O Configuration*1	24 digital input lines, 22 digital output lines 1 high-speed counter (pulse/dir or A/B) 1 PWM/PTO output (pulse/dir)
Extention Interfaces	I²C, SPI, FlexBus, GPIO
FPGA Options	Lattice LFE2-6 or Lattice LFE2-20
PLD	MACH XO 640 (CPLD)
OS Support	Linux, eCos*2
Programming	IEC 61131-3 and C/C++
HMI Options	driver for dot-matrix display and 4x4 keypad
Operating Temperatur	-40°C to +85°C
Dimensions	70 x 41,5 x 7,8 (LxWxH, in mm)

1. Represents the default I/O configuration at time of delivery. The I/O configuration may be changed by the user (Driver Development Kit required).
2. eCos available as extension to the development kit. No PLCcore option for eCos available.

Releated Products

PLCcore-5484
ECUcore-5484 with pre-integrated IEC 6113-3 runtime kernel, CiA 302/405 compliant CANopen Manager and Shared Process Image API.

Driver Development Kit
Provides all necessary source code and API reference documentation for own user-specific I/O driver development based on the ECUcore-5484.

Target Applications

Communication Gateways

Industrial Controls

High-speed Data Acquisition

SYS TEC ELECTRONIC

Development Kit

- ECUcore-5484 Development Board
- ECUcore-5484 System On Module mounted on the Development Board
- International power supply, 12VDC, 1500mA
- RS232 cable, 1.8m
- FTP patch cable Cat.5e, 2.0m
- CAN cable for 5 nodes, incl. 2x 120Ω termination plugs
- Leverage tool
- ESD handling instructions
- VMware image with Linux cross-development toolchain for ECUcore-5484

Included with Development Kit PLCcore-5484:

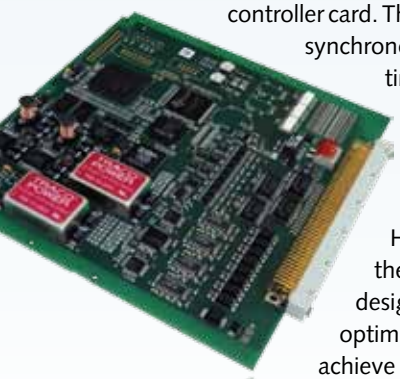
- OpenPCS - IEC 61131-3 Programming Environment for Windows
- Shared process image reference application project in source code

Driver Development Kit (DDK)

The Driver Development Kit for ECUcore-5484 is required for designing user-specific I/O level drivers to match with own application carrier boards. The DDK contains the following components:

- VHDL project for PLD or FPGA including all necessary files to create new PLD/FPGA software (VHDL source files, pin assignment, timing settings, project file etc.)
- Sourcecode for Linux kernel driver (pc5484drv.ko) with all necessary files to generate a new kernel driver module (C and H files, Makefiles etc.)
- Sourcecode for Linux user-library (pc5484drv.so) with all necessary files to create a new user library module (C and H files, Makefiles etc.)
- PLD programming tool (flashpld + plddrv.ko) Allows for updating the software running on the PLD and FPGA
- I/O driver reference demo application (iodrvdemo) in source code

Application Success Story



For an OEM customer, SYS TEC electronic developed a ruggedized motion controller card. The controller is programmable in C/C++ and supports synchronous operation of up to 8 axes within a 50µs cycle time. It was especially designed and optimized for use in embedded motion control applications that operate under harsh environmental conditions, such as often present in off-road mobile machinery. The design is based on the ECUcore-5484 SOM. However, in order to ensure reliable operation under the specified parameters, the ECUcore-5484 was designed onto the application board. A performance-optimized multi-CPU design approach was chosen to achieve a 50µs synchronization cycle. This consist of the 32-bit ECUcore-5484 based Supervisory CPU circuitry, a digital signal processor (DSP) for control loop calculations and two FPGA for handling the I/O processing. All CPU's are connected by a bus system. The Supervisory CPU executes the user-application backed by an eCos real-time OS.

Ordering Informations

4001000	ECUcore-5484
KIT-157	Development Kit ECUcore-5484
SO-1098	Driver Develeopment Kit ECUcore-5484
3390045	PLCcore-5484, FPGA20
3390035	PLCcore-5484, FPGA6
3390005	PLCcore-5484, PLD
KIT-153	Development Kit PLCcore-5484

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广州虹科电子科技有限公司 广州市五山华南理工大学国家科技园 2 号楼 504-505 室（510640）
电话： 020-3874 4528; 3874 4538 e-mail: sales@hkaco.com 网站：www.hkaco.com