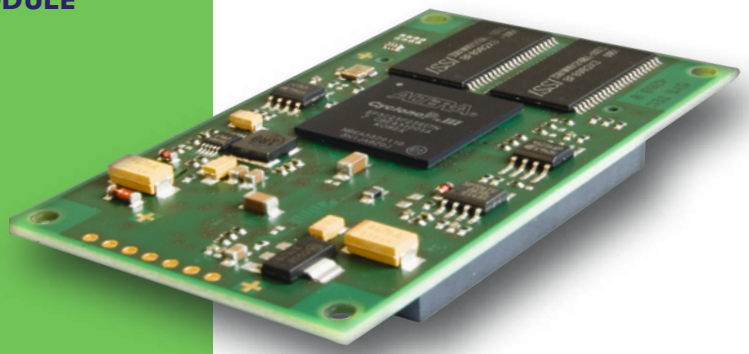
ECUcore-EP3C

INSERT-READY FPGA CORE MODULE



VHDL and C/C++ programmable

2 Ethernet PHYs

Customizable board connector pinout

Open Source Ethernet POWERLINK Technology

Order Information

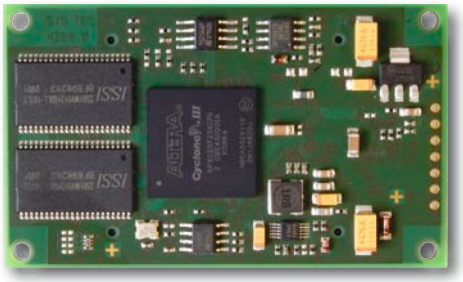
ECUcore-EP3C module:	4001018
Development Kit:	KIT-161

System on Module with Cyclone III and NIOS II 32-Bit Soft IP Processor

The ECUcore-EP3C System on Module (SOM) is an extremely compact, product-ready hardware and software solution that accelerates embedded Ethernet POWERLINK designs.

Based on ALTERA's Cyclone III EP3C25 FPGA the ECUcore-EP3C offers essential features for embedded real-time networking applications. Two Ethernet PHYs directly wired to the FPGA are available on-board.

IP core components required to build own Ethernet POWERLINK applications, such as the Ethernet MAC (openMAC), HUB (openHUB) and the POWERLINK protocol stack (openPOWERLINK) are available as open source under BSD license.



Furthermore the ECUcore-EP3C comes equipped with 2 MiB SRAM, 1 MiB Serial Flash for application storage and a 32 kiB EEPROM on a compact PCB form factor with simplified 64-pin board-connector layout for easy integartion into application-specific carrier boards.

With the ECUcore-EP3C SYS TEC extends the flexibility of existing SOM solutions to the silicon layer. With using an FPGA instead a fixed microcontroller the functionality of the core and the corresponding board layout is now "re-programmable" by the developer. The board provides up to 31 pins to implement custom functions such as DIO, PWM, SPI bus or Data Address Bus.

The ECUcore-EP3C is aimed at OEM and ODM who intend to extend existing product designs with Ethernet POWERLINK. Here, the Development Kit ECUcore-EP3C provides an excellent platform to evaluate the functionality of POWERLINK and begin with application development right on a product-ready SOM.

Technical Specification ECUcore-EP3C

ON-BOARD HARDWARE CONFIGURATION

- ALTERA Cyclone III FPGA (EP3C25) core with 24624 Logic Elements and 4 PLLs
- 1 MiB Flash
- 2 MiB SRAM
- 32 kiB EEPROM
- Reset unit with voltage monitoring
- 50 MHz on-board oscillator
- PCB dimensions: 70 mm x 42 mm

DEFAULT I/O CONFIGURATION

- 31 freely programmable User I/Os

EXTERNAL BUS INTERFACES

- Two 10/100 Mbps Fast Ethernet on–board PHYs wired to FPGA via RMII or full MII
- 1 JTAG
- SPI, Ethernet MAC, Data Address Bus, UART available as IP core

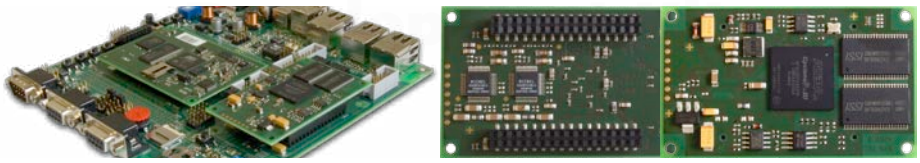
OPERATING CONDITIONS

- Temperature: -40 °C to +85 °C
- Humidity: 10 to 90% (non-condensing)

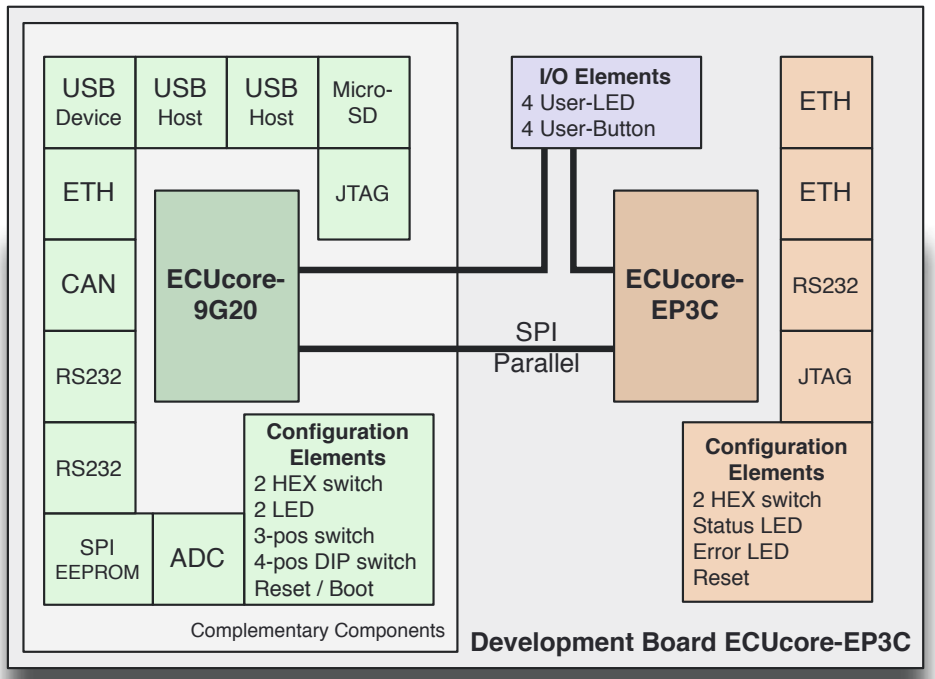
Designed for

Embedded real-time Industrial Ethernet applications.

The ECUcore-EP3C



The ECUcore-EP3C Development Kit is a low-cost, high-performance method of evaluating the ALTERA Cyclone EP3C FPGA and ECUcore-EP3C System on Module (SOM). The Kit includes the ECUcore-EP3C, an application carrier board, and accessories required to immediately begin development work. The FPGA on the ECUcore-EP3C is pre-programmed with a stand-alone openPOWERLINK demo application running on a NIOS II Soft CPU. Besides the Soft CPU the FPGA configuration includes a seamlessly integrated openMAC, openHUB and the required system peripherals. The demo application achieves a POWERLINK timing of 400 µs cycle time, about 1 µs Poll Response latency and less than 1 µs synchronization jitter.



ECUcore-EP3C :: Highlights

- Low-cost development kit
- FPGA, memory and support circuitry integrated in an insert-ready SOM
- Ready to run Board Support Package with openPOWERLINK reference application
- Core software components openPOWERLINK, openMAC with Auto-Response feature and openHUB available as open source under BSD license
- Customizable board connector pinout
- Scalable functionality and performance
- Extremely compact PCB form factor (70mm x 42mm)

Extended Board Configuration

The development board comes with an extra socket and all components necessary to populate and operate the ARM9 based ECUcore-9G20 with Linux OS in addition to the ECUcore-EP3C. The two SOM are connected through parallel or serial bus lines (selectable via Jumper). This extended board configuration allows for evaluating and developing Multi-CPU applications where the ECUcore-9G20 acts as host-CPU and the ECUcore-EP3C implements the communication processor.

Kit Contents

HARDWARE

- Development board ECUcore-EP3C with:
  - One ECUcore-EP3C socket and one ECUcore-9G20
  - One Status and Error LED wired to ECUcore-EP3C
  - Two HEX-encoding switch wired to ECUcore-EP3C and two HEX-encoding switches wired to ECUcore-9G20
  - Two RJ45 Ethernet sockets wired to ECUcore-EP3C and one RJ45 Ethernet socket wired to the ECUcore-9G20
  - One RS-232 connector wired to ECUcore-EP3C and two RS-232 connectors wired to the ECUcore-9G20
  - Micro SD card socket wired to the ECUcore-9G20
  - One USB device connector (type B) and two USB host connectors (type A) wired to the ECUcore-9G20
  - Two JTAG interfaces, one wired to ECUcore-EP3C (USB-Blaster compatible) and one wired to ECUcore-9G20 (ICE)
  - One CAN bus connector (SUB-D9)
  - Four push-button and four LED user I/O wired to both ECUcore via Jumper
  - Four bit DIP-switch and 3-pos slider wired to the ECUcore-9G20
  - Input voltage range 9 ... 24 V DC
- ECUcore-EP3C SOM
- USB-JTAG adapter for use with ECUcore-EP3C and Altera Quartus II IDE
- RS-232 cable, jumpers and leverage tool
- Power supply adapter 12V DC/1.5A

SOFTWARE

- Altera Quartus® II design software
- openPOWERLINK reference application in source code and project files
- openPOWERLINK protocol stack source code
- FPGA project files for reference implementation (openMAC, openHUB, RAM infrastructure, NIOS II framework)
- Wireshark Ethernet Monitor with POWERLINK plug-in
- openPOWERLINK Live-CD with POWERLINK Managing Node application for x86 PCs

DOCUMENTATION

- Quick Start Guide
- openPOWERLINK Reference Manual
- Hardware Manual ECUcore-EP3C
- Hardware Manual Development Board
- Development Board schematics

Release 04/2010 - Subject to change without prior notice.

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